ADVACAM
Imaging the Unseen

ADVAPIX

TPX3

Synchronization Guide

Model No.: APXT3M-Xxx200128
APXT3M-Xxx201030

Synchronization operation

Timepix3 detector can measure precise Time of Arrival and Time over Threshold (Energy).

For the operation it requires an external 40 MHz clock.

a) External triggering

When the AdvaPIX TPX3 is used in standalone mode, this clock is supplied from the readout itself. To synchronize a single AdvaPIX TPX3 device with an external device, an external 40 MHz synchronization clock must be connected to **CLK P/N** pins.

b) Synchronization of multiple detectors

To synchronize multiple AdvaPIX TPX3 devices with each other without an external system, the 40 MHz clock can be supplied from one of the devices (called master device) by interconnecting the devices with a synchronization cable.

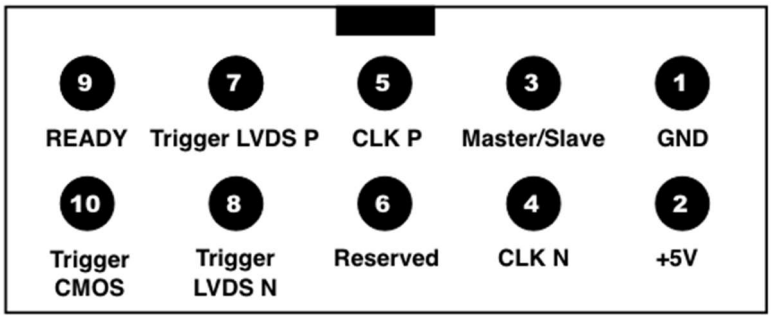
The **Master/Slave** pin selects whether the device outputs the 40 MHz clock on CLK P/N pins when **Master/Slave** is set to master (not connected). When the **Master/Slave** pin is selected to slave (connected to 1 – 5 V), the device expects the 40 MHz clock as input on the CLK P/N pins.

There is one Trigger connections on AdvaPIX TPX3 – **Trigger LVDS P/N** The **Master/Slave** pin controls the sense of the trigger pins. If the device is master, the trigger pins are output – Trigger OUT. If the device is slave, the trigger pins are input – Trigger IN.

With the proper clock on **CLK P/N** pins the device measurement can be started by the pulse on Trigger pin. The level or edge of the signal the device should react on can be setup in the software (see below). The device will accept trigger signal when the measurement is setup in trigger mode, and it has been started – the device goes to wait for trigger mode. This is signaled by the **READY** pin – when in logical 1 (2,5 V), the device is ready to accept the trigger signal.

When the device is setup as master, the trigger pins are working as Trigger Out - a signal that shows when the device is measuring. When the shutter is open the signal is in logical 0. When not measuring it is in logical 1.

Synchronization connector pinout



Pin	Name	Description
1	GND	Connected to the device ground.
2	+5V	Connected to the device +5 V power supply. *Do not load this pin more than 50mA.*
3	Master/Slave	Selects if the device is master (Open) or slave (1 - 5V)
4	CLK N	Input / Output external 40 MHz clock, M-LVDS, negative polarity.
5	CLK P	Input / Output external 40 MHz clock, M-LVDS, positive polarity.
6	RESERVED	*Reserved.* Do not connect any signals to this pin.
7	Trigger LVDS P	Trigger input (slave) or output (master), M-LVDS positive polarity.
8	Trigger LVDS N	Trigger input (slave) or output (master), M-LVDS negative polarity
9	Ready	CMOS (0-2.5V), output signal, in logical 1 means that the device is ready to accept trigger signal, logical 0 - device is not ready.
10	Trigger CMOS	*Reserved.* Do not connect any signals to this pin.

External triggering requirements

Only some devices are capable of external triggering functionality!
Please, carefully check compatibility requirements listed below.
Use of incompatible hardware might cause permanent damage!

1. The device model number is APXT3M-Xxx200128 or APXT3M-Xxx201030.
2. The device can be used **ONLY** with M-LVDS input signal, CMOS is not supported.
3. The device **MUST** be in **SLAVE mode** (Pin 3 [Master/Slave] connected to pin 2 [+5 V]).
4. **External** 40 MHz reference clock **MUST** be provided on M-LVDS input.
5. The M-LVDS bus **must be terminated externally** in proximity (less than 2 cm) of (last) detector unit on synchronization signals harness. Failure to terminate the bus with 100 Ω termination resistor will result in signal integrity problems resulting in intermittent operation or failure of detector synchronization.
6. Synchronization pulse requirements:
    a. Minimum pulse width: 150 ns.
    b. Maximum repetition frequency of the synchronization pulse is limited by measurement mode, number of registered events (in Pixels mode) and connected HW.

If your application requires use of **5 V TLL or 3,3 V LVCMOS** trigger signal, please contact our technical support team. We provide our customers with reference design and adapter board for converting the input signals to comply with above mentioned requirements upon customer request.

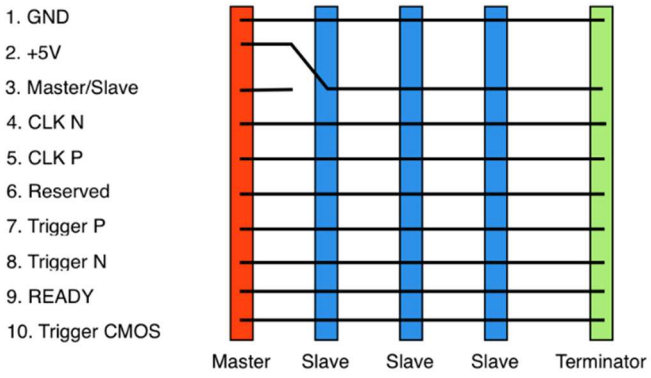
If you have any questions, please do not hesitate to contact technical support at support@advacam.cz

Synchronization of multiple detectors

Cable connections

Synchronization connection example (see below) for 4 synchronized AdvaPIX TPX3 detectors without synchronization unit (1 set as master, 3 as slave). 10 horizontal black lines represent single ribbon cable connection diagram.

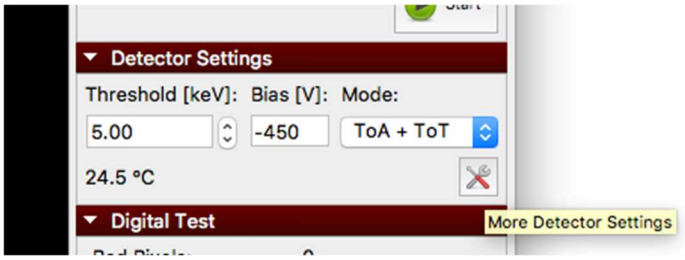
0,05” ribbon cable with differential impedance close to 100 Ω must be used for the synchronization harness.



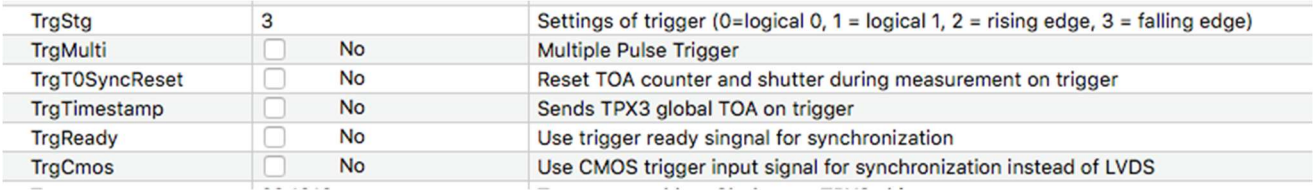
LVDS signals (CLK and Trigger) need to be resistor terminated to function correctly!
For ribbon cable termination resistor value is 120 Ω.
Synchronization cable and terminator is supplied on costumer request.

Synchronization parameters in the software

The parameters of synchronization (Trigger in level/edge, etc.) can be setup in Pixet software. In the main window on Detector Settings panel → More Detector Settings icon open the More detector Settings dialog:



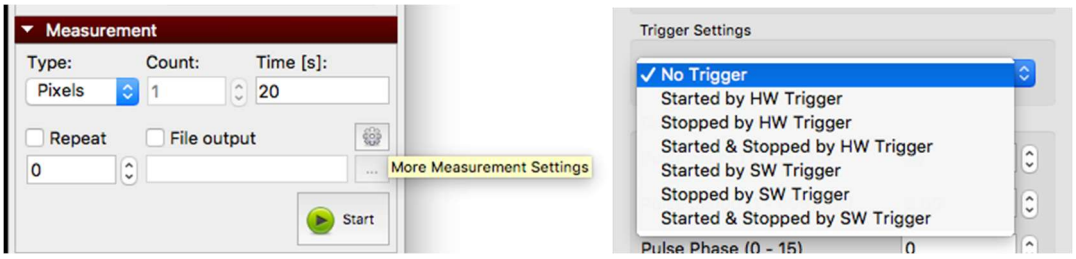
In the readout tab the synchronization parameters can be set:



Parameter	Description
TrgStg	Sets the edge / level of the input trigger signal the device reacts on
TrgMulti	When yes, the master devices sends periodically trigger signal during measurement. (For debugging purposes and synchronization verification.)
TrgT0SyncReset	If yes, when the trigger signal arrives and the shutter is already open, it will reset the internal time counter (ToA) to zero.
TrgTimestamp	If yes, when the device receives trigger signal when the shutter is open, it will request current timestamp from the Timepix3. This is for debugging and synchronization verification.
TrgReady	If yes, the ready signal will be used during synchronization – the master device will wait for all devices to be ready before asserting the trigger signal. In order to work, must be enabled for all devices on the synchronization cable.
TrgCmos	Selects which of the trigger pins is used – if yes, Trigger CMOS is used, if no, Trigger LVDS P/N

Synchronization measurement

To perform synchronized measurement with multiple AdvaPIX TPX3 devices or triggered by external signal, the trigger measurement must be setup in the software. To enable the triggers, open in main window, Measurement panel -> More Measurement Settings and in Trigger Settings select one of the trigger options:



For AdvaPIX TPX3, only No Trigger and Started by HW Trigger options are available.

- **No Trigger** – normal measurement, without synchronization
- **Started by HW Trigger** – when the device measurement is started (clicking on START button) the device waits for trigger signal

When multiple AdvaPIX TPX3 devices needs to be started in synchronous mode and the Ready parameter is set to No, first, the slave devices must be started in trigger mode and the master device last. The master device is selected by the synchronization cable. To know, which device is master, go to More Detector Settings -> Readout:

If Ready is set to Yes, the order in which the devices are started does not matter. For the measurement in frame mode, the Ready parameter must be enabled.

SW settings for using external triggering

More Detector Settings

	Master
TrgReady	No
TrgStg	0-3
TrgT0SyncReset	Yes or No
Other trg parameters	No

More Measurement Settings

	Master
Trigger Settings	Started by HW trigger

SW settings for synchronization of multiple detectors

More Detector Settings

	Master	Slave
TrgReady	Yes	Yes
TrgStg	0	3
Other trg parameters	No	no

Measurement Settings

	Master	Slave
Trigger Settings	Started by HW trigger	Started by HW trigger

Release history

Date	Changes	Changed by
19/08/27	First version	
21/09/27	New device version; Document Format	
24/04/29	Synchronization requirements added	J. Baborák
24/05/24	New graphic style of the document	J. Baborák, P. Bloudek
24/05/31	Synchronization pulse requirements added	J. Baborák, M. Konečný
24/06/11	Examples of SW settings added	J. Baborák

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